REMARKS/ARGUMENTS

STATUS OF CLAIMS

In response to the Office Action dated April 8, 2008, claims 1 and 2 have been amended. Claims 1-6, 9-17, 20, 23, 27 and 29-31 are now pending in this application. No new matter has been added. Claims 7, 8, 18, 19, 21, 22, 24-26 and 28 have been withdrawn from consideration as being directed to non-elected species.

Claims 1 and 2 have been amended to recite "gate conductor functions for writing to, and erasing and reading from the semiconductor ***storage*** device..." to provide consistency. The claim amendments are non-narrowing claim amendments.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 1, 2 and 3 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

With respect to claim 1, the Examiner maintains that there is insufficient antecedent basis for "gate conductor" in line 10.

With respect to claim 2, the Examiner maintains that there is insufficient antecedent basis for "gate conductor" in line 11.

With respect to claim 3, the Examiner maintains that there is insufficient antecedent basis for "gate conductor" in line 16.

The rejections are respectfully traversed.

The third line of each of claims 1 and 2 and the seventh line of claim 3 recite "a gate conductor..." In addition, what is being recited in line 10 of claim 1, line 11 of claim 2 and line 16 of claim 3 is "gate conductor functions"; i.e., functions of the gate

conductor (that has been earlier recited). Since this is the initial recitation of "gate conductor functions" and the gate conductor to which this refers has been earlier recited in each of these claims, there is sufficient antecedent support for "gate conductor" in "gate conductor functions". Therefore, withdrawal of this rejection under 35 U.S.C. § 112, second paragraph, is respectfully solicited.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102 AND § 103

I. Claims 1, 6, 9-11, 13, 16 and 29 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shukuri (US 2006/0008992).

Claims 2, 23 and 30 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shukuri (US 2006/0008992).

Claims 3, 4, 5, 17, 27 and 31 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shukuri (US 2006/0008992).

That is, claims 1-6, 9-11, 13, 16, 17, 23 and 29- 31 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shukuri (US 2006/0008992). However, in view of the Examiner's comments regarding claim 12 on page 3 of the Office Action, it is believed that the Examiner intended claims 1-6, 9-13, 16, 17, 23 and 29-31 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shukuri (US 2006/0008992).

The rejections are respectfully traversed.

Each of independent claims 1, 2 and 3 of the present application requires, *inter alia*, a single gate electrode for a gate conductor and that gate conductor functions for writing to, and erasing and reading from each semiconductor storage device/memory element are solely carried out with the single gate electrode.

The Examiner has referred to Figs. 46-65 Shukuri as having gate conductor 123 and that it consists of single gate electrode 123. However, Applicant cannot accept the Examiner's interpretation of Shukuri as being reasonable. In the embodiments of Shukuri (Figs. 46-65) that have (i) memory function bodies formed on opposite sides of the gate electrode (claim 1), (ii) charge storage regions in a shape of a film parallel to a surface of the semiconductor layer and existing over part of the channel region and part of the corresponding diffusion region, and straddling a boundary therebetween (claim 2) and (iii) memory function bodies formed so as to extend along the word line on opposite sides of the word line (claim 3), there is a gate conductor that has a split gate configuration, **NOT** a gate conductor consisting of single gate electrode, as required by each of independent claims 1-3.

Furthermore, gate conductor functions for writing to, and erasing and reading from each semiconductor storage device/memory element of Shukuri can not be ***solely*** carried out by control gate 123, as memory gate 127 is needed. In this regard, Figs. 48-51 of Shukuri show the different voltages for left/right memory gates (MGL/MGR) and control gates (CG) for erase operation, write operation, read operation for plus direction and read operation for reverse direciton.

While control gate 123 inherently fuctions for writing to, and erasing and reading from each semiconductor storage device/memory element, this different from what is recited in independent claims 1-3 that gate conductor functions for writing to, and erasing and reading from each semiconductor device/memory element are ***solely*** carried out with the single gate electrode. Therefore, independent claims 1-3, as well as dependent claims 4-6, 9-13, 16, 17, 23 and 29-31, are patentable over Shukuri.

II. Claims 14, 15 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Shukuri (US 2006/0008992).

However, claims 14, 15 and 20 depend directly or indirectly from independent claim 1. Therefore, claims 14, 15 and 20 are also patentable over Shukuri.

III. In view of the above, the allowance of claims 1-6, 9-17, 20, 23, 27 and 29-31 is respectfully solicited.

CONCLUSION

In view of the above, applicant(s) believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Edward J. Wise (Reg. No. 34,523) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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